

BOX AF



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Michael R. Flannery et al.

Title:

INTEGRATED CIRCUIT WITH UNIFIED INPUT DEVICE, MICROPROCESSOR AND DISPLAY SYSTEMS

Docket No.: Filed: 450.202US1 July 1, 1999

Due Date: April 15, 2002

Examiner:

Jose R. Diaz

Group Art Unit: 2815

Serial No.: 09/346,283

BOX AF

Commissioner for Patents Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

 \underline{X} A return postcard.

X An Amendment and Response Under 37 CFR 1.116, including Clean Version of Pending Claims (7 Pages).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 50-0439.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: BOX AF, Commissioner for Patents, Washington, D.C. 20231, on this day of March, 2002.

Candis B. Buending

Name

Signature

Customer Number 21186

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(GENERAL)

DITED PROCEDURE - EXAMINING GROUP 2815

S/N 09/346,283

PATENT

Group Art Unit: 2815

STATES PATENT AND TRADEMARK OFFICE Examiner: Jose R. Diaz

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MICROPROCESSOR AND DISPLAY SYSTEMS

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box AF Commissioner for Patents Washington, D.C. 20231

In response to the final Office Action mailed January 15, 2002, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect the amendment of previously pending claims 1 and 4-6. The specific amendments to individual claims are detailed in the following marked up set of claims.

- (Twice Amended) An integrated circuit with a micromechanical element comprising a 1. semiconductor support substrate supporting a sensor element, a logic circuit and a semiconductor visual display element, the sensor element electrically connected to the logic circuit, and the logic circuit being electrically connected to the semiconductor visual display element[, said sensor element for providing an input to said logic circuit in response to a mechanical actuation of said sensor element].
- The integrated circuit of claim 1 wherein said visual display (Twice Amended) 4. element comprises an array of semiconductor pixels having [diameter] pitch dimensions of less than 20 micrometers.